## REMARKS

### Status of Claims

Claims 1 to 29 remain in the application.

### Claim Amendments

Independent claims 1 and 16 have been amended to clarify the functionality of the second parallel code multiplying operation in light of the specification and for strict antecedent support. Specifically, claims 1 and 16 have been amended to recite in part: "multiplying the M symbols by each of the L codewords of the second set of codewords ...[and] ... multiplying the set of N consecutive first output symbols by each of the K codewords of the ~~second~~first set of codewords". Please note that these amendments were not made in response to the prior art, but were only made for the sake of clarity.

Prior to the foregoing amendments, claims 1 and 16 recited that **both** the first parallel code multiplying operation **and** the second parallel code multiplying operation included multiplying by each of the codewords of the **second code**. This was clearly and obviously an inadvertent wording in light of the remainder of the specification that was not apparent to the Applicant until after the final rejection was issued, which is the reason why this amendment was not earlier presented.

The terms "the first code" and "the second code" have been replaced with "the first set of codewords" and "the second set of codewords", respectively, throughout the claims for strict antecedent support.

Independent claims 1 and 16 have been further amended to clarify that the "overall maximum of the second output symbols output of said second parallel code multiplying operations" is an "overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operations".

**Claim Rejections – 35 U.S.C. 103**

In the final rejection, the Examiner maintains the rejection of claims 1, 9, 13, 14, 16, 24, 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over United States Patent No. 5,550,809 ("Bottomley") in view of United States Patent No. 5,204,874 ('Falconer"). In response, Applicant respectfully submits that the currently amended claims are both novel and inventive over Bottomley and Falconer, both alone and in combination, for at least the reasons stated below.

The law on obviousness under 35 U.S.C. 103 was recently addressed in ***KSR Int'l v. Teleflex, Inc.***, *No. 04-1350, slip op. at 14 (U.S., Apr. 30, 2007).* Following this, examination guidelines were released on October 10, 2007 in regards to determining obviousness under 35 U.S.C. 103. According to these guidelines, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in ***Graham v. John Deere Co.*** *383 U.S. 1,148 USPQ 459 (1966).* Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court are as follows:

(1) Determining the scope and content of the prior art;

(2) Ascertaining the differences between the claimed invention and the prior art; and

(3) Resolving the level of ordinary skill in the pertinent art.

The Graham factors, including secondary considerations when present, are the controlling inquiries in any obviousness analysis. Once the findings of fact are articulated, Office personnel must provide an explanation to support an obviousness rejection under 35 U.S.C. 103. According to KSR, for the Patent Office to properly combine references in support of an obviousness rejection, the Patent Office must identify a reason why a person of ordinary skill in the art would have sought to combine the respective teachings of the applied references.

Applicant's analysis below demonstrates that the Examiner has failed to properly conform to the aforementioned guidelines for a finding of obviousness under 35 U.S.C. 103.

Claim 1

Applicant submits that claim 1 of the present application is patentable over Bottomley and Falconer, as the findings of fact as articulated by the Examiner are inaccurate. In particular, the Examiner has not properly determined the differences between the claimed invention and the prior art. Furthermore, the Examiner has not provided a valid explanation to support an obviousness rejection under 35 U.S.C. 103. Applicant's reasoning is detailed below.

*Differences between the claimed invention and the prior art*

Claim 1, as amended, recites "for each set of M consecutive symbols, performing a first parallel code multiplying operation by multiplying the M symbols by each of the L codewords of the second set of codewords, thereby producing L first output symbols, each of the L output first output symbols being associated with one of the L codewords" (emphasis added). Therefore, claim 1 defines a first parallel code multiplying operation for each set of M consecutive symbols. The Examiner contends that Bottomley teaches this subject matter in column 1, lines 25-34. However, this portion of Bottomley teaches "at a transmitter, a binary information symbol b (±1) can be spread by multiplying b with a spreading sequence x; for example, the spreading sequence x might be +1, -1, +1, -1, consisting of four binary chips". Applicant previously pointed out that by describing the spreading of only one binary information symbol, Bottomley is completely silent to a first parallel code multiplying operation as claimed by the Applicant. In particular, there is no hint or suggestion of any parallelism in the spreading of the binary information symbol.

In the final rejection, the Examiner's response to Applicant's previous argument on this point states that "[the foregoing portion of Bottomley] suggests that each binary information symbol is spread by multiplying by a spreading sequence (i.e. set of chips "+1,-1,+1,-1") meaning there is more than one multiplication being performed simultaneously (i.e., parallel)". However, Applicant submits that this statement by the Examiner is entirely inaccurate, as the multiplication of the binary information symbol b by the spreading sequence x taught by Bottomley represents a single multiplication, i.e., multiplication of a single symbol by a single sequence. Spreading in conventional Code Division Multiple Access (CDMA) systems, which is what Bottomley refers

to in the passage cited by the Examiner, does not include a first parallel code multiplying operation, as in the claimed invention, i.e multiplying M consecutive symbols by each of the L codewords of a second set of codewords in parallel.

Furthermore, it should be noted that the portion of Bottomley that the Examiner has relied upon clearly refers to an encoding process, i.e., "at a transmitter ... multiplying b with a spreading sequence x" (emphasis added), while Applicant's claims recite a method and an apparatus for decoding M x N symbols.

Currently amended independent claim 1 also recites "for a set of N consecutive first output symbols associated with the codeword, performing a respective second parallel code multiplying operation by multiplying the set of N consecutive first output symbols by each of the K codewords of the first set of codewords to produce a set of K second output symbols, each second output symbol being associated with one of the K codewords and with said codeword of the set of said L codewords" (emphasis added). Therefore, claim 1 defines a second parallel code multiplying operation that multiplies N consecutive output symbols from the first parallel code multiplying operation by each of the codewords of the first set of code words in parallel.

In the final rejection, the Examiner contends that column 1, lines 25-34 of Bottomley also teaches the second parallel code multiplying operation recited in unamended claim 1, which, as noted above, contained an inadvertent technical error, whereby it was erroneously stated that the second parallel code multiplying operation involved multiplying by the second code. Applicant respectfully submits that Bottomley certainly does not describe a second parallel code multiplying operation that multiplies the set of N consecutive first output symbols by each of the K codewords of the first set of codewords, as recited in currently amended claim 1.

Furthermore, as noted above, column 1, lines 25-34 of Bottomley does not teach or suggest a parallel code multiplying operation whatsoever, nor does it teach a "first parallel code multiplying operation" in combination with a "second parallel code multiplying operation", as claimed by the Applicant.

If the Examiner intends to continue to rely on Bottomley for allegedly having disclosed a "first parallel code multiplying operation" in combination with a "second parallel code

multiplying operation" in the claimed manner, the Examiner is requested to identify a specific portion of Bottomley that teaches this, as column 1, lines 25-34 of Bottomley, which the Examiner has relied on to date in rejecting the unamended claims, teaches only the spreading of a single binary information by a single spreading sequence.

The Examiner concedes that Bottomley does not teach "determining an overall maximum of the second output symbols output of said second parallel code multiplying operations". Applicant agrees with the Examiner. Moreover, Applicant submits that Bottomley has little or nothing to do with the present Application. Furthermore, as noted above, the independent claims have been amended to clarify that the "overall maximum" is an "overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operations". Applicant submits that Bottomley fails to teach or even suggest determining an overall maximum second output symbol of the second output symbols output, as claimed.

In view of the Examiner's admitted difference between claim 1 of the present application and Bottomley, the Examiner looks to Falconer at column 6, lines 10-14 to contend that claim 1 of the present application is obvious. Applicant appreciates that this portion of Falconer teaches that "The predetermined size of the block of data symbols defined by the matrix is derived from the maximum number of data symbols which can be transmitted at a predetermined chip rate within a predetermined length transmission block" (emphasis added). However, the "size of the block of data symbols" represents the number of data symbols, which has nothing to do with determining an overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operations, as claimed by the Applicant.

In the final rejection, the Examiner argues that "determining an overall maximum of the second output symbols output of said second parallel code multiplying operations," as previously recited in independent claim 1, "when interpreted by the examiner given the broadest most reasonable interpretation in light of the applicant's specification as written, may be understood as the total amount of data symbol output" (emphasis added). However, Applicant submits that the Examiner's suggested interpretation could not possibly be reasonably arrived at in light of the specification as written, particularly in light of, for example, passages such as those found at page 11, lines 6-10 and page 13, lines 7-10, which clearly describes the selection/determination of an

overall maximum second output symbol, not the selection/determination of how many second output symbols there are. Nonetheless, in order to potentially expedite prosecution, independent claims 1 and 16 have been amended to clarify that the "overall maximum" is an "overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operations", as noted above. Applicant respectfully submits that the Examiner's erroneous interpretation of the previously recited "overall maximum" is clearly not reasonable in light of the currently amended claims, as determining a number of data symbols, as taught by Falconer, cannot be equated to determining an overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operations, as claimed.

In view of the foregoing, Applicant submits that the Examiner has not properly determined the differences between the claimed invention and the prior art. Therefore, the findings of fact as articulated by the Examiner are improper.

*Explanation to support an obviousness rejection*

As noted above, for the Patent Office to properly combine references in support of an obviousness rejection, the Patent Office must identify a reason why a person of ordinary skill in the art would have sought to combine the respective teachings of the applied references. The examination guidelines indicate that "The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." The Court quoting In re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), stated that " '[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.''' Applicant appreciates that the Examiner has articulated a reason why the claimed invention would have been obvious. However, for reasons detailed below, the Examiner's articulated reason can not be regarded as being valid.

The Examiner has again stated that 'it would have been obvious for one of ordinary skill in the art at the time of the Applicant's invention to include, "determining an overall maximum of the second output symbols output of said second parallel code multiplying operations," in the invention as disclosed by Bottomley et al. for the purposes of data rate control.' However, as

noted above, Falconer does not teach "determining an overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operations". Furthermore, Applicant maintains that even if Falconer were to teach this feature, which Applicant does not concede, there is no apparent reason as to why the person skilled in the art would understand that combining this feature with Bottomley would facilitate data rate control.

The Examiner has argued that one skilled in the art would understand that column 6, lines 10-14 of Falconer relates to data rate control and would therefore conceive of combining this teaching of Falconer with the teaching of Bottomley since "'determining an overall maximum of the second output symbols output of said second parallel code multiplying operations," can be interpreted as dealing with the amount of symbol output.' However, the Examiner has not shown that combining Bottomley and Falconer in the suggested manner would have the benefit suggested by the Examiner, i.e., facilitating data rate control. In addition, the currently amended claims recite determining/selecting "an overall maximum second output symbol", which Applicant submits precludes the Examiner's erroneous interpretation of the previously recited determining/selecting "an overall maximum".

Furthermore, the particular portions of Bottomley and Falconer that the Examiner has relied on, namely "at a transmitter ... multiplying b with a spreading sequence x" (column 1, lines 25-34 of Bottomley; emphasis added) and "The predetermined size of the block of data symbols defined by the matrix is derived from the maximum number of data symbols which can be transmitted at a predetermined chip rate within a predetermined length transmission block" (column 6, lines 10-14 of Falconer; emphasis added), are clearly directed to features of a transmitter and have absolutely nothing to do with a method and apparatus for decoding M x N symbols, as claimed.

Furthermore, Applicant notes that even if the Patent Office is able to articulate and support a suggestion to combine the references, it is impermissible to pick and choose elements from the prior art while using the application as a template—see ***In re Fine***, 837 F.3d 1071 (Fed. Cir. 1988). It is respectfully submitted that incorporating the teachings of Falconer in relating to the size of the block of data symbols with the teachings of Bottomley is an attempt to arrive at claim 1 while using the present application as a template. This attempt is flawed

because the Examiner's proposed modification does not account for the fact that neither Falconer nor Bottomley teach Applicant's claimed "first parallel code multiplying operation" and "second parallel code multiplying operation".

If one were to use the present application as a template, which is nonetheless improper according to ***In re Fine***, one would have to first modify Bottomley so that it teaches Applicant's claimed "first parallel code multiplying operation" together with Applicant's claimed "second parallel code multiplying operation". Also, one would have to modifying Falconer so that it teaches "determining an overall maximum second output symbol of the second output symbols output of said second parallel code multiplying operation" as claimed by the Applicant. These numerous modifications cannot be regarded as obvious because the gap between the prior art and the claimed invention is too great. Applicant notes that the aforementioned examination guideline that issued on October 10, 2007 indicates that "the gap between the prior art and the claimed invention may not be 'so great' as to render the [claim] non-obvious to one reasonably skilled in the art." Therefore, the proposed combination of Bottomley and Falconer cannot render the present application obvious.

In view of the foregoing, Applicant submits that claim 1 of the present application is patentable over Bottomley and Falconer.

Applicant submits that claims 9, 13, 14, 16, 24, 27 and 28 are patentable over Bottomley and Falconer for similar reasons provided above in respect of claim 1.

The Examiner is respectfully requested to reconsider and withdrawn the rejections of claims 1, 9, 13, 14, 16, 24, 27 and 28 under 35 U.S.C. 103(a).

**Other Claim Rejections – 35 U.S.C. 103(a)**

The Examiner rejects claims 2, 4, 5, 8, 17, 19, 20, 23, 25 and 26 under 35 U.S.C. 103(a) as being unpatentable over Bottomley in view of Falconer and further in view of United States Patent No. 5,103,459 ("Gilhousen"). Applicant notes that the aforementioned claims depend on one or more claims for which their rejections should be withdrawn. Therefore, Applicant submits that the rejection of claims 2, 4, 5, 8, 17, 19, 20, 23, 25 and 26 should similarly be

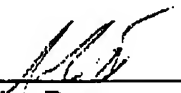
withdrawn. The Examiner is respectfully requested to reconsider and withdraw the rejection of claims 2, 4, 5, 8, 17, 19, 20, 23, 25 and 26 under 35 U.S.C. 103(a).

Favorable consideration is requested.

In the event that that the Examiner has concerns regarding the present response, the Examiner is encouraged to contact the undersigned at the telephone listed below.

Respectfully submitted,

LEGNAIN, ABDELGADER ET AL.



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